UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/933,492	08/20/2001	David R. Hembree	00-0625.1	6973

22823 7590 05/24/2005

STEPHEN A GRATTON
THE LAW OFFICE OF STEVE GRATTON
2764 SOUTH BRAUN WAY
LAKEWOOD, CO 80228

EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 05/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/933,492	HEMBREE ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *52 - 62 and 70 - 77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *52 - 62 and 70 - 77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/25/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 25, 2005 has been entered. An action on the RCE follows.

Response to Amendment

2. Applicant's amendment filed on April 25, 2005 has been received and entered in the case.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 52 – 62 and 70 – 77 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 52, 56, 60 and 70, it is unclear what the applicant regards as:

(a) Regarding the limitation "a plurality of conductors... in electrical communication with the component contacts configured to redistribute the

component contacts on the good components" how is the plurality of conductors configured to redistribute the component contacts on the good components?

(b) Regarding the limitation "and to repair the defective component by connecting selected component contacts on the defective component with selected integrated circuits on the defective component;" it is not clear how a defective component may be repaired by connecting the defective component with other integrated circuits on the defective component. The limitation states that the component is itself defective, so how can it be repaired by connecting to itself?

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 52 – 62 and 70 – 77 are rejected under 35 U.S.C. 102(e) as being anticipated by Hsuan et al.

Regarding claims 52, 60 and 70, as best as understood by the Examiner, Hsuan et al. discloses in e.g., Fig. 1, Fig. 5, Fig. 6 and column 6, lines 1 – 34 a semiconductor component comprising:

- a substrate (semiconductor wafer 100 in Fig. 2) comprising a plurality of semiconductor components (semiconductor IC dice 102; column 4, line 57), each component including a plurality of component contacts (114; column 4, lines 57 – 58) and a plurality of integrated circuits (Integrated circuits, i.e., 110a, 110b, etc in Fig. 4) in electrical communication (by using the element 112) with the component contacts (114; see Fig. 4), the components including a plurality of good components (any dice 102 that are good dice in Fig. 2) and at least one defective component (any defective die in Figs. 5 and 6; column 6, lines 29 – 33) identified during a component testing process (first testing process; column 5, lines 48 – 63); and
- a metal redistribution layer (claim 70; the metal redistribution line 134a or 134b; column 6, lines 25 – 28) on the substrate (100) comprising a plurality of conductors (136 and 140) on the components in electrical communication with the component contacts (114; see Fig. 6) configured to redistribute the component contacts on each component (column 6, lines 25 – 28), to electrically connect the contacts (114) on components (102; see Fig. 6), to either repair, reconfigure, or electrically isolate the defective component, or to electrically connect multiple components in a cluster that excludes the defective component (claim 70; column 5, lines 54 – 63 and column 6, lines 4 – 53), and to repair the defective component by connecting selected component contacts on the defective component with selected integrated circuits on the defective component (column 5, lines 54 – 63), and to reconfigure the component contacts (by redistribution lines 134a and 134b) on the defective component (claim 60; column 6, lines 25 – 34).

Furthermore, the limitations "a component testing process in which digital data represents locations of the good components, the defective component and the component contacts" and "the conductors having a pattern corresponding to the digital data" are product-by-process limitations. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 53, Hsuan et al. discloses in e.g., Fig. 1, Fig. 5, Fig. 6 and column 6, lines 1 – 34 the components including a second defective component (a second bad die from the bad dies; column 6, lines 33 – 34) and the conductors are configured to electrically isolate the second defective component (claim 53; column 3, lines 8 – 15).

Regarding claim 54, Hsuan et al. discloses in e.g., Fig. 1, Fig. 5, Fig. 6 and column 6, lines 1 – 34 the components (102) including a second defective component (a second bad die

from the bad dies; column 6, lines 33 – 34) and the conductors (136 and 140) being configured to reconfigure the component contacts on the second defective component (column 5, lines 54 – 63).

Regarding claim 55, Hsuan et al. discloses in e.g., Fig. 1, Fig. 5, Fig. 6 and column 6, lines 1 – 53 the components including a second defective component (a second bad die from the bad dies; column 6, lines 33 – 34) and the conductors being configured to electrically connect multiple components in a cluster (wafer level IC) that excludes the second defective component (column 6, lines 11 – 53).

Regarding claim 56, as best as understood by the Examiner, Hsuan et al. discloses in e.g., Fig. 1, Fig. 5, Fig. 6 and column 6, lines 1 – 34 a semiconductor component comprising:

- a substrate (semiconductor wafer 100 in Fig. 2) comprising a plurality of components (semiconductor IC dice 102; column 4, line 57), a plurality of component contacts (114; column 4, lines 57 – 58);
- the components (102) including a plurality of good components (e.g., any one of the good elements 102) and at least one defective component (any defective die in Figs. 5 and 6; column 6, lines 29 – 33) identified during a component testing process (first testing process; column 5, lines 48 – 63);
- a plurality of conductors (136 an d140) on the components configured to redistribute the component contacts (114) on the good components (any dice 102 that are good dice in Fig. 2) and to electrically isolate the component contacts on the defective component (column 7, lines 19 – 30) on the substrate during burn-in testing of the good components (column 6, lines 44 – 53).

Furthermore, the limitations "a component testing process in which digital data represents locations of the good components, the defective component and the component contacts" and "the conductors having a pattern corresponding to the digital data" are product-by-process limitations. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 57, Hsuan et al. discloses in e.g., Fig. 1, Fig. 5, Fig. 6 and column 6, lines 1 – 34 a plurality of terminal contacting (balls on the element 140; column 6, line 55) on the good components (good 102s) in the selected patterns in electrical communication with the conductors (e.g., 140).

Regarding claim 58, Hsuan et al. discloses in e.g., Fig. 1, Fig. 5, Fig. 6 and column 6, lines 1 – 34 the conductors (136 and 140) being configured to electrically connect a plurality of

good components in a cluster (wafer level IC) that exclude the defective component (column 6, lines 11 – 53).

Regarding claim 59, Hsuan et al. discloses in e.g., Fig. 1, Fig. 5, Fig. 6 the substrate (100) comprising a semiconductor wafer (100; column 4, line 52), and the components (102) comprising semiconductor dice or semiconductor packages (die-IC; column 6, lines 4 – 10).

Regarding claim 61, Hsuan et al. discloses in e.g., Fig. 1, Fig. 5, Fig. 6 and column 6, lines 1 – 34 a plurality of terminal contacts (balls on the element 140; column 6, line 55) on the good components (102) in electrical communication (by using the element 112) with the conductors (136 and 140) and the component contacts (114; see Fig. 6) on the good components.

Regarding claims 62 and 76, Hsuan et al. discloses in e.g., Fig. 1, Fig. 5, Fig. 6 and column 6, lines 1 – 34 the substrate (100) comprising a semiconductor wafer (100) or portion thereof and the components (102) comprising a semiconductor dice (die-IC; column 6, lines 4 – 10).

Regarding claim 71, Hsuan et al. discloses in e.g., Fig. 1, Fig. 5, Fig. 6 and column 6, lines 1 – 34 the good components include a plurality of terminal contacts (balls on the element 140; column 6, line 55) in electrical communication with the component contacts on the good components (column 6, lines 53 – 55).

Regarding claim 72, Hsuan et al. discloses in e.g., Fig. 1, Fig. 5, Fig. 6 and column 6, lines 1 – 34 the component contacts (114) comprising bond pads (column 4, lines 52 – 53).

Regarding claim 73, Hsuan et al. discloses in e.g., Fig. 1, Fig. 5, Fig. 6 and column 6, lines 1 – 34 the conductors (136 and 140) on the good components have a fan out configuration (see Fig. 6).

Regarding claim 74, Hsuan et al. discloses in e.g., Fig. 1, Fig. 5, Fig. 6 and column 6, lines 1 – 34 the substrate (100) comprising a semiconductor wafer (column 4, line 52).

Regarding claim 75, Hsuan et al. discloses in e.g., Fig. 6 and column 6, lines 1 – 34 a protective layer (132a) on the conductors (136 and 140) on the good components.

Regarding claim 77, Hsuan et al. discloses in e.g., Fig. 6 and column 6, lines 1 – 34 the components (102) including a second defective component (a second bad die from the bad dies; column 6, lines 33 – 34) and the conductors being configured to electrically isolate the second defective component (column 6, lines 11 – 53).

Response to Arguments

7. Applicant's arguments with respect to claims 52 – 62 and 70 – 77 have been considered but are moot in view of the new grounds of rejection by different interpretation of the previously applied reference.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
Thursday, May 12, 2005

GEORGE ECKERT
PRIMARY EXAMINER